UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION, and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. CV 08-00877 PSG **DECLARATION OF DAVID MAY IN SUPPORT OF PLAINTIFFS' SUPPLEMENTAL CLAIM CONSTRUCTION BRIEFING** **[RELATED CASES]**
HTC CORPORATION, and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. CV 08-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. CV 08-05398 PSG

I, David May, do hereby declare as follows:

1. I have been retained by Plaintiffs HTC Corporation and HTC America, Inc. to provide expert testimony relating to claim construction issues. More specifically, I have been asked to comment on how one of ordinary skill in the art would understand the term "instruction register" as recited in claims of U.S. Patent No. 5,440,749.

2. I am an expert in computer science and the design and implementation of microprocessors. I graduated in Computer Science from King''s College Cambridge in 1972. I have been a Professor of Computer Science at the University of Bristol in United Kingdom since 1995 and served as the head of the Computer Science department from 1995 to 2006. I have more than 30 years of experience in microprocessor design and implementation. I am named in more than 45 patents in the area of microprocessors and multiprocessing systems. I am a founder and currently serve as the Chief Technology Officer of XMOS Semiconductor, a company that designs and creates processors for digital electronics, hardware development tools and other products. I was also previously employed by Inmos, a British semiconductor company based in Bristol, where I served as the lead architect and designer of the Transputer microprocessors. In 1990, I received an Honorary Doctor of Science from the University of Southampton, followed in 1991 by my election as a Fellow of The Royal Society of London and the award of the Patterson Medal of the Institute of Physics in 1992. In 2010, I was elected a Fellow of the Royal Academy of Engineering in the U.K. Attached as Exhibit A is a copy of my curriculum vitae.

3. As noted above, I have been asked to provide my expert opinion regarding how one of ordinary skill in the art at the time of the '749 patent's filing would understand "instruction register" as recited in claims of the '749 patent after reviewing the patents' specification and relevant portions of the prosecution history, which I have done. Based on my review, I understand that during the prosecution of the '749 patent, the examiner noted in a written summary of an in-person interview regarding claim 1 of that patent, "operand width is variable and right adjusted," in reference to an effort by the applicants to distinguish the Boufarah prior art reference (U.S. Patent No. 5,127,091). I have also been asked to explain what it means for an operand to be "variable width" and "right adjusted," and to provide the technical context in the

'749 patent for this statement.

4. By way of background, microprocessors typically operate by executing what are known as "instructions," each instruction directing a microprocessor to perform a specific operation. Microprocessors typically provide numerous instructions for performing different types of mathematical and logical operations. Most microprocessors, for example, include one or more instructions for performing addition or subtraction.

5. The operation to be performed by an instruction is normally specified in the instruction by an operation code, or "opcode." The values on which the specified operation is performed are commonly referred to as "operands." This terminology is similar to that used to describe arithmetic expressions such as (5 + 3), in which the operator is "+" and the two operands are the values "5" and "3."

6. While the opcode is always part of an instruction, the operand may be held in memory, in registers, or may be part of the instruction itself. The term "register" here refers to a storage device in the microprocessor that holds information, such as a value. For instance, in a hypothetical instruction "ADD r3, 5" that adds a constant value "5" to the variable value held in a register "r3," the opcode would be "ADD," and the two operands would be the constant value "5" and the variable value held in the register "r3."

7. The term "instruction register" is commonly understood as a storage device that is used to hold one or more instructions and to supply those instructions to the circuits of the microprocessor that will interpret and execute them. An instruction register may be of different widths (i.e., number of bits). A "bit" in computer science is a unit of information that specifies a value of either 1 or 0, and the term "byte" refers to a unit of information that includes 8 bits. The specification of the '749 patent, for example, discloses an instruction register that can hold up to 32 bits (4 bytes) of instructions (*i.e.*, a 32-bit instruction register). In the case of the '749 patent, an instruction may consist simply of an opcode represented in 8 bits (one byte) and perform operations on an operand held in registers. That means that up to four 8-bit instructions can be fetched at once from memory to the 32-bit instruction register. An instruction in the '749 patent may also consist of both an opcode and an operand.

8. Depending on the design of the microprocessor, the "operand," if held in an instruction along with the opcode, may be of different widths (sizes), *e.g.*, 8 bits, 16 bits or 24 bits, and could be positioned in different places within the instruction register. As explained below, however, the '749 patent requires that the operand be "right justified" in the instruction register such that the same opcode can be used with operands of different widths.

9. The term "right justified" refers to the fact that an operand in an instruction is always positioned in the "right side" of the instruction register. The following three figures below demonstrate this concept. In each of these examples, a 32-bit (4 byte) instruction register such as the one described in the '749 patent is broken into four bytes of eight bits each, which are shown side-by-side from left to right. Each of the three examples below shows an "operand" of a different width that is always located in the right-most bits of the instruction register:

Examples of "right justified" operands in a 32-bit instruction register

Right justified 8-bit (1 byte) operand:

8 bits	8 bits	8 bits	8 bits
Opcode	Opcode	Opcode	**Operand**

Left bit 32-bit Instruction Register Right bit

In the example above, the 32-bit instruction register contains two 8-bit instructions, each of which has only an 8-bit opcode without any operand, and a 16-bit instruction with an 8-bit opcode and an 8-bit operand that is positioned in the "right side" of the instruction register.

Right justified 16-bit (2 byte) operand:

8 bits	8 bits	8 bits	8 bits
Opcode	Opcode	**(part of the) Operand**	**(part of the) Operand**

Left bit 32-bit Instruction Register Right bit

In the example above, the 32-bit instruction register contains one 8-bit instruction, which has only an 8-bit opcode without any operand, and a 24-bit instruction with an 8-bit opcode and a 16-bit operand that is positioned in the "right side" of the instruction register.

Right justified 24-bit (3 byte) operand:

8 bits	8 bits	8 bits	8 bits
Opcode	**(part of the) Operand**	**(part of the) Operand**	**(part of the) Operand**

Left bit 32-bit Instruction Register Right bit

In the example above, the 32-bit instruction register contains one 32-bit instruction with an 8-bit opcode and a 24-bit operand that is positioned in the "right side" of the instruction register.

10. As shown by the three examples above, an operand, if held in an instruction, can be of varying width. Because the microprocessor needs the entire operand to execute the instruction correctly, it needs to be able to determine where the operand begins and ends – in other words, the width of the operand. One common approach in microprocessor design is to use a different opcode for each possible operand length.

11. To take one example, a common instruction in microprocessors and the one described in the '749 patent (discussed below) is known as a "JUMP" instruction. A JUMP instruction typically tells the microprocessor to begin executing instructions from a portion of memory, or an "address" (*i.e.*, location in the memory), different from the address of the current instruction. In the prior art systems discussed in the '749 patent, the length of the operand may vary depending on the opcode used to represent the JUMP instruction. A JUMP instruction may, for example, tell the microprocessor to move to a target address that is close to, or far away from, the address of the current instruction. This "jump" can be achieved by a shorter or longer operand, respectively, to specify the desired target address for the JUMP instruction. In either case, the "opcode" must specify both the JUMP instruction and the width of its corresponding operand, *e.g.*, 8, 16 or 24 bits. The opcode, for example, would need to tell the microprocessor, "this is a JUMP instruction and the opcode length is 16 bits." The obvious disadvantage of this approach is that, in this example, three separate opcodes would be required for the same JUMP operation to account for three possible operand lengths.

12. The "right justified" instruction register in the '749 patent avoids this issue by

placing all of the bytes of the operand (up to 3) on the right-side of the instruction register, and placing the opcode of the instruction immediately to the left of the operand bytes, as shown in the figures above. Execution of the instructions proceeds from left-to-right of the instruction register, causing the opcode to be encountered first. The operand is then obtained by simply reading it from the right-most bits of the instruction register. Because the operands are "right justified" and therefore always located in the same place in the instruction register, there is no need to rely on the opcode to determine the operand width. The '749 specification explains that this "right justified" approach allows the same opcode to be used regardless of the length of the operand:

> Variable Width Operands
>
> Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. 20 shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

('749, 18:34-56 (underlining supplied by me).)

13. The requirement that the operands be right justified in the instruction register, as would be understood by a person skilled in the art at the time of the filing of the application for the '749 patent, aims to provide a simplified, high-performance microprocessor design. The variable length operands are needed to provide an efficient representation of programs and to enable several instructions to be fetched at the same time. Unless these operands are right-justified in the instruction register, the microprocessor circuitry will be more complicated to account for the potentially differing locations of the operands within the instruction register,

contrary to the stated aims of the alleged invention of the '749 patent.

14. In my opinion as a person skilled in the art, the prosecution history also supports this understanding of the "instruction register" of the '749 patent. I understand that a written summary of an in-person interview with the examiner on October 25, 1994 in the '749 patent's prosecution history mentions that the applicants attempted to distinguish U.S. Patent No. 5,127,091 to Boufarah. I understand that, in this summary, the examiner noted with respect to claim 1: "operand width is **variable** and **right adjusted**." 10/25/1994 Interview Summary at 1 (Chen Decl., Ex. 19, Examiner Interview Summary Record, Docket Item No. 316-20.) (emphasis added). One of ordinary skill in the art would understand the examiner's statement to be referring to the fact that the instruction register in the '749 patent holds variable-length and right-justified operands. The interview summary is thus consistent with the specification's description of the instruction register. It is therefore my opinion that the specification and file history of the '749 patent make clear that the operands in the "instruction register" claimed in the '749 patent must be variable width and right-justified.

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I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Executed on the 12th day of September, 2012, in Bristol, United Kingdom.

M David May

David May

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CERTIFICATE OF SERVICE

I am a citizen of the United States and a resident of the State of California. I am employed in Santa Clara County, State of California. I am over the age of eighteen years, and not a party to the within action. My business address is Cooley LLP, Five Palo Alto Square, 3000 El Camino Real, Palo Alto, California 94306-2155.

On September 14, 2012, I served **DECLARATION OF DAVID MAY IN SUPPORT OF PLAINTIFFS' SUPPLEMENTAL CLAIM CONSTRUCTION BRIEFING** in the manner described below:

☐ (BY U.S. MAIL) I am personally and readily familiar with the business practice of Cooley LLP for collection and processing of correspondence for mailing with the United States Postal Service, and I caused such envelope(s) with postage thereon fully prepaid to be placed in the United States Postal Service at Palo Alto, California.

☐ (BY MESSENGER SERVICE) by consigning the document(s) to an authorized courier and/or process server for hand delivery on this date.

☐ (BY FACSIMILE) I am personally and readily familiar with the business practice of Cooley LLP for collection and processing of document(s) to be transmitted by facsimile and I caused such document(s) on this date to be transmitted by facsimile to the offices of addressee(s) at the numbers listed below.

☐ (BY OVERNIGHT MAIL) I am personally and readily familiar with the business practice of Cooley LLP for collection and processing of correspondence for overnight delivery, and I caused such document(s) described herein to be deposited for delivery to a facility regularly maintained by _____ for overnight delivery.

☒ (BY ELECTRONIC MAIL) I am personally and readily familiar with the business practice of Cooley LLP for the preparation and processing of documents in portable document format (PDF) for e-mailing, and I caused said documents to be prepared in PDF and then served by electronic mail to the parties listed below.

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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 14th day of September, 2012, at Palo Alto, California.

/s/Kyle D. Chen

Kyle D. Chen